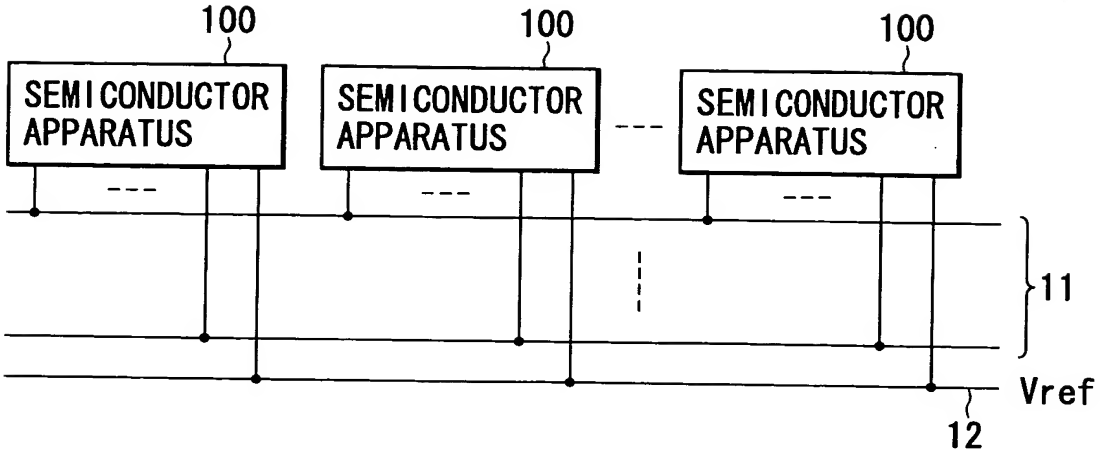


FIG. 1 (PRIOR ART)

FIG. 2
(PRIOR ART)

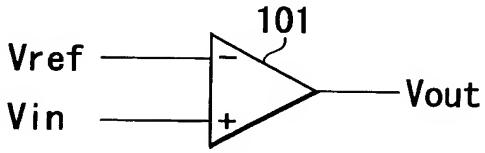
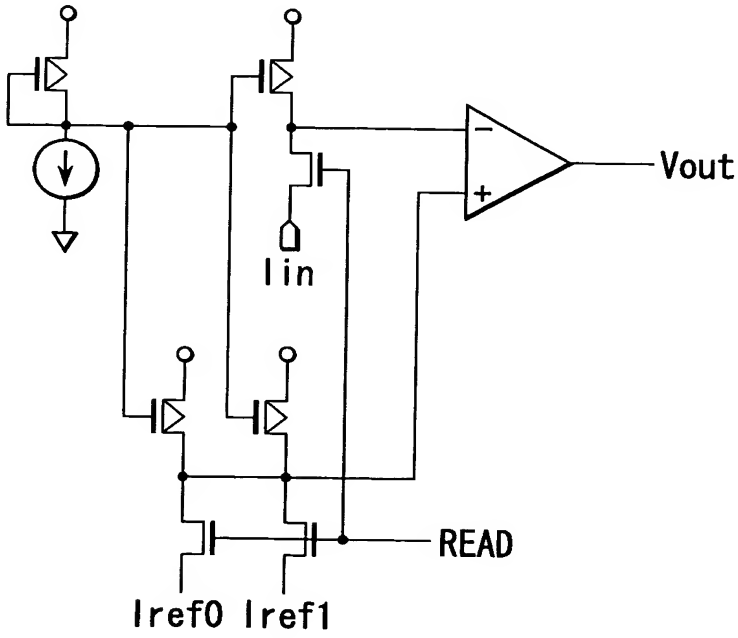


FIG. 3
(PRIOR ART)



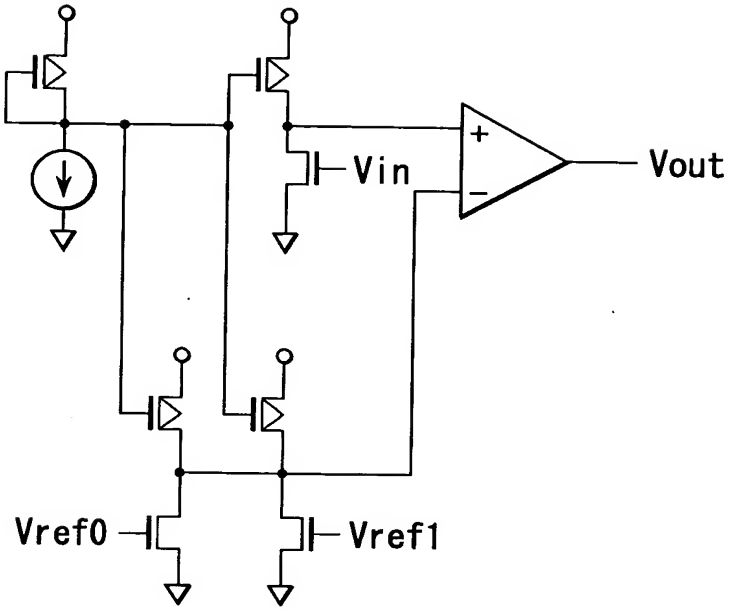


FIG. 4 (PRIOR ART)

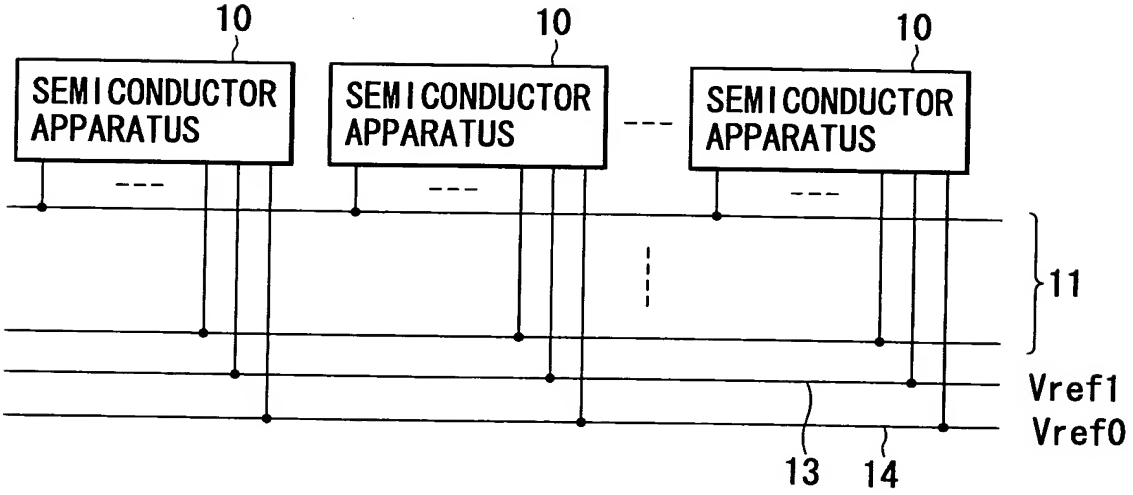


FIG. 5

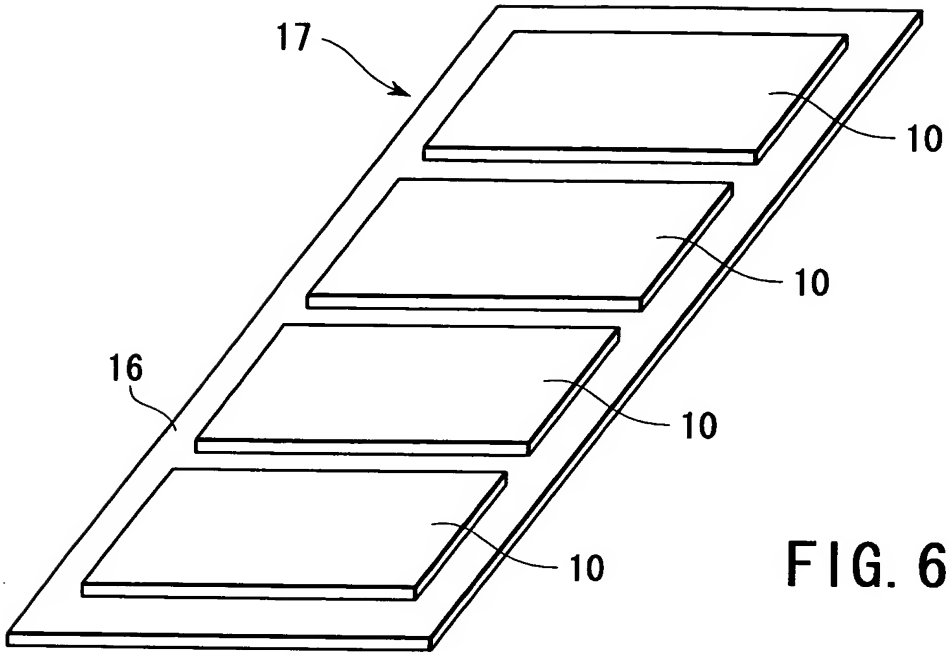

17
10
10
16
10
10

FIG. 6

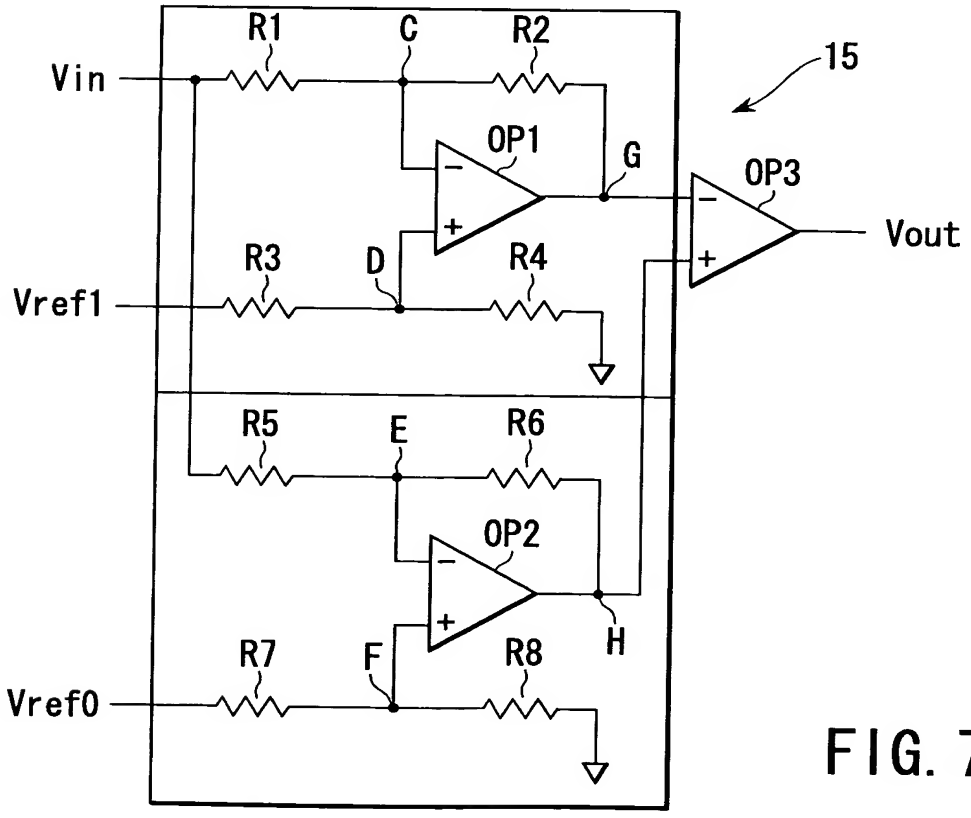

R1
C
R2
15
Vin
OP1
G
OP3
Vout
R3
D
R4
Vref1
R5
E
R6
OP2
H
R7
F
R8
Vref0

FIG. 7

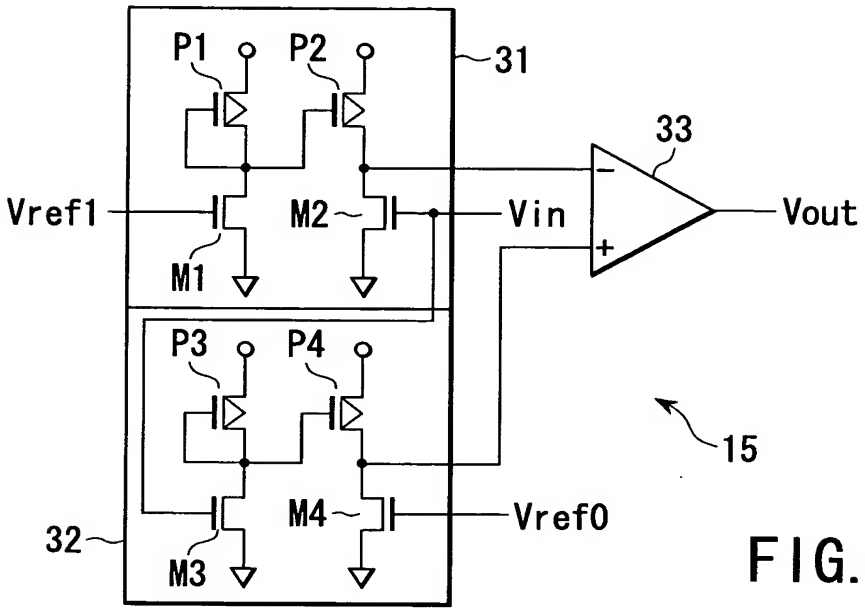

P1
P2
31
33
Vref1
M2
Vin
Vout
M1
P3
P4
15
M4
Vref0
32
M3

FIG. 8

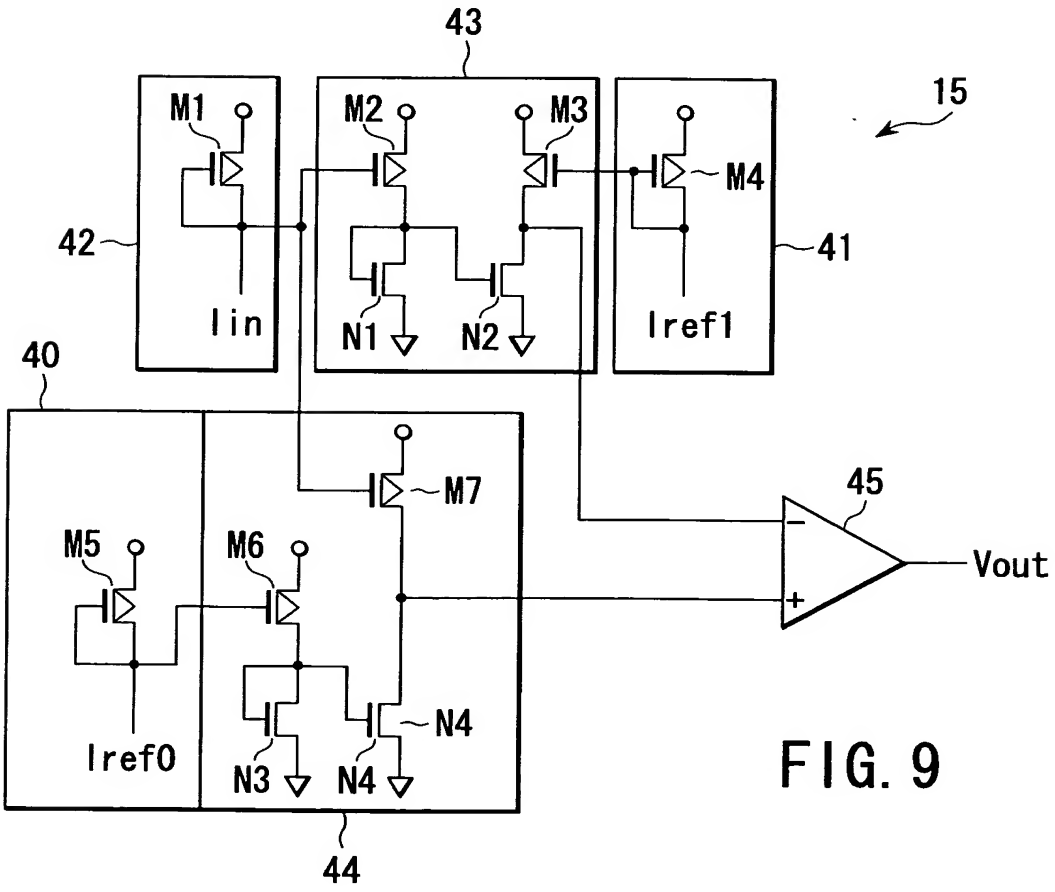

43
15
M1
M2
M3
M4
42
41
Iin
N1
N2
Iref1
40
M7
45
M5
M6
Vout
N4
Iref0
N3
N4
44

FIG. 9

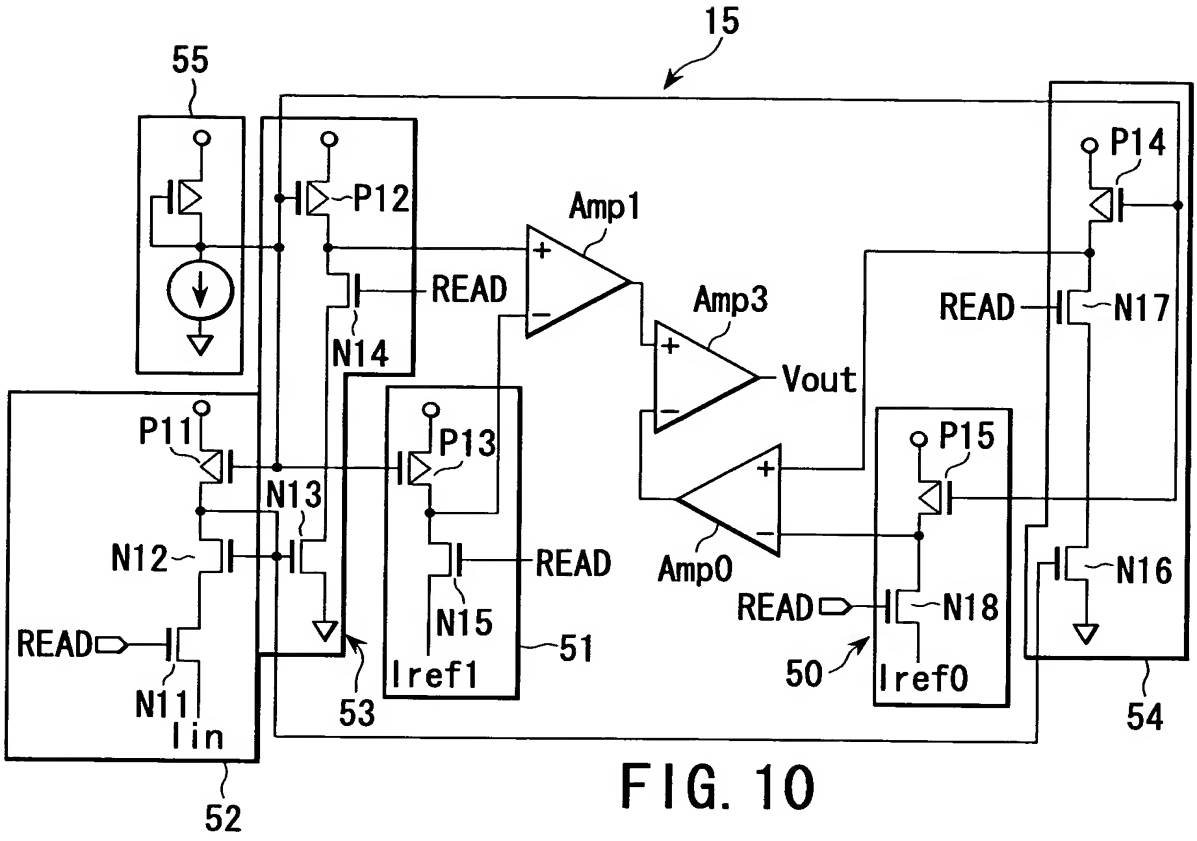

15
55
P12
Amp1
READ
N14
Amp3
Vout
P14
READ
N17
P11
P13
N13
N12
READ
READ
N15
Amp0
P15
N16
READ
N18
N11
Iin
53
Iref1
51
50
Iref0
54
52

FIG. 10

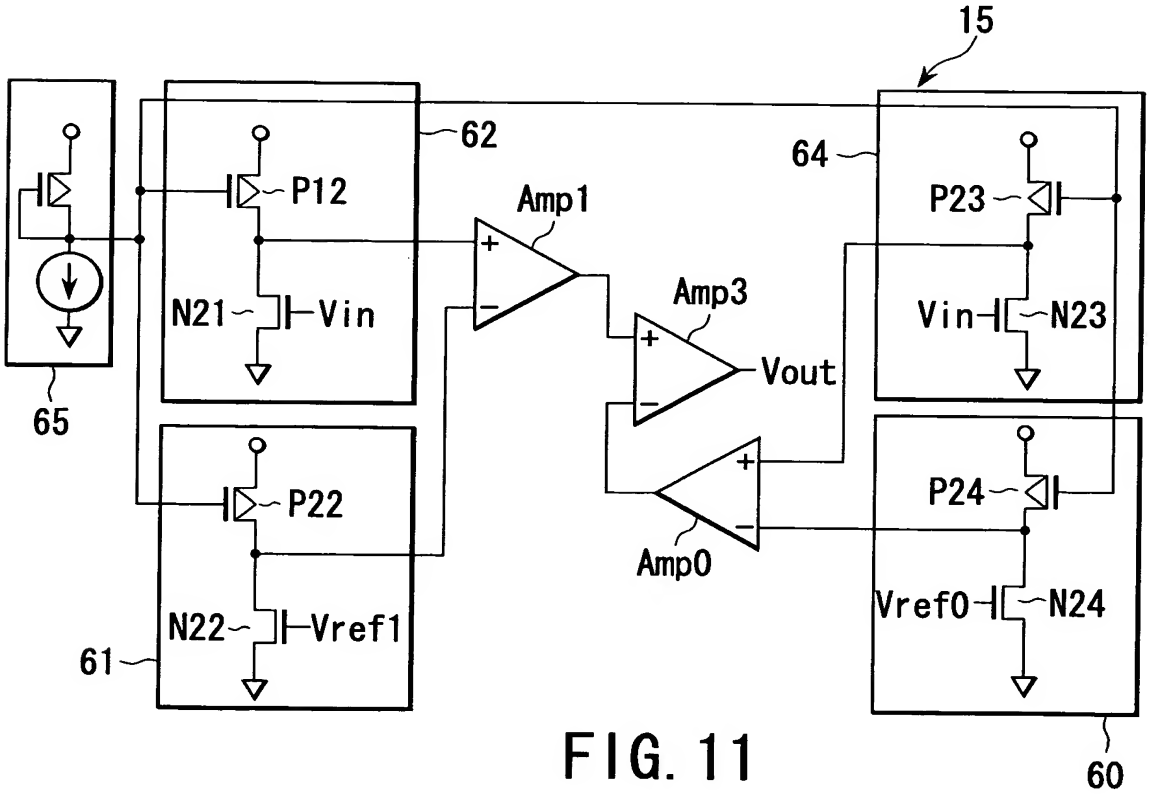

15
62
64
P12
Amp1
P23
N21
Vin
Amp3
Vout
Vin
N23
65
P22
P24
Amp0
N22
Vref1
Vref0
N24
61
60

FIG. 11

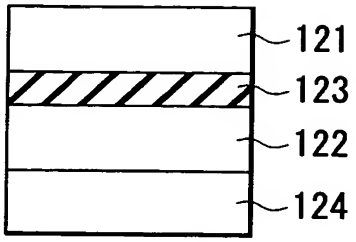
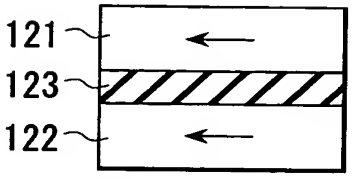
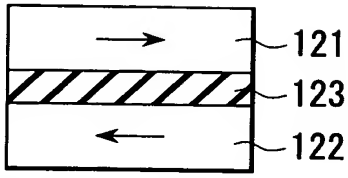


FIG. 12



PARALLEL
(SMALL RESISTANCE)

FIG. 13A



INVERSELY PARALLEL
(LARGE RESISTANCE)

FIG. 13B

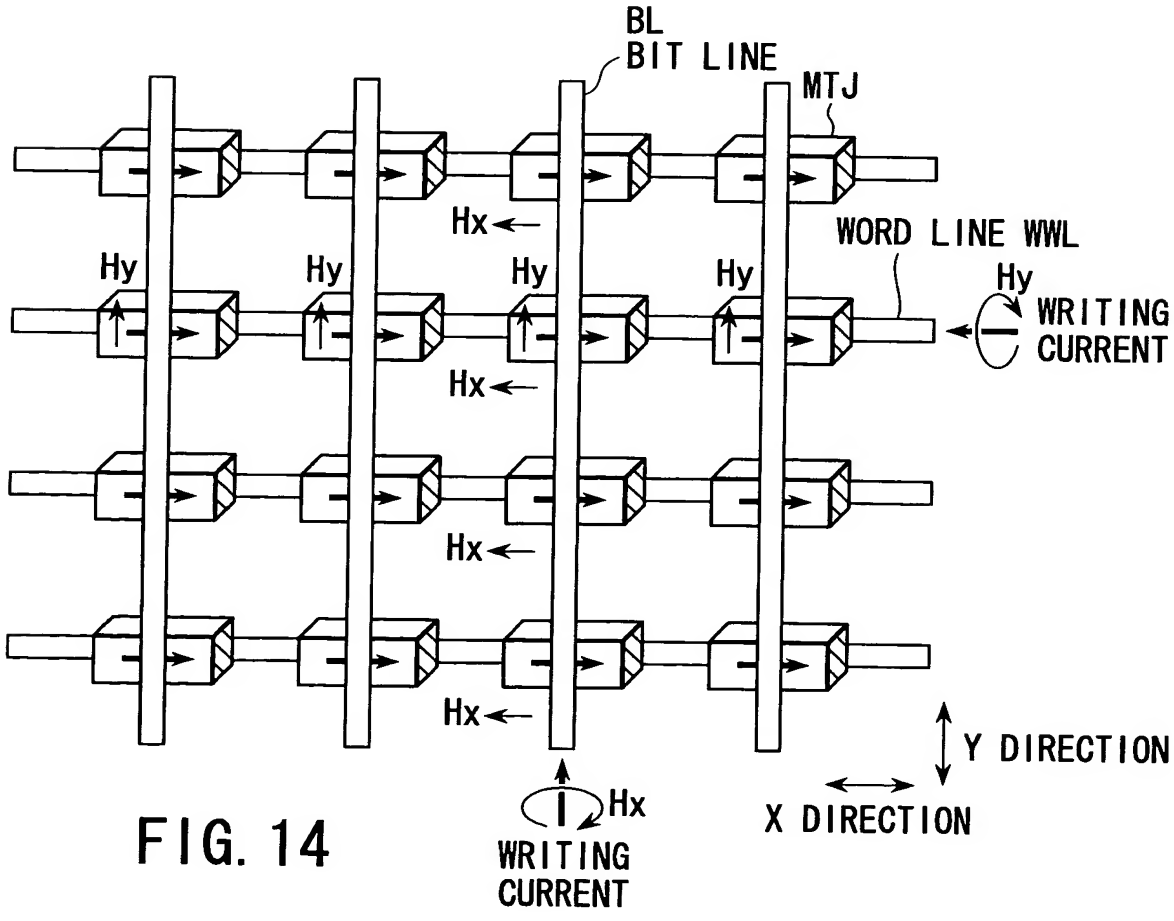


FIG. 14

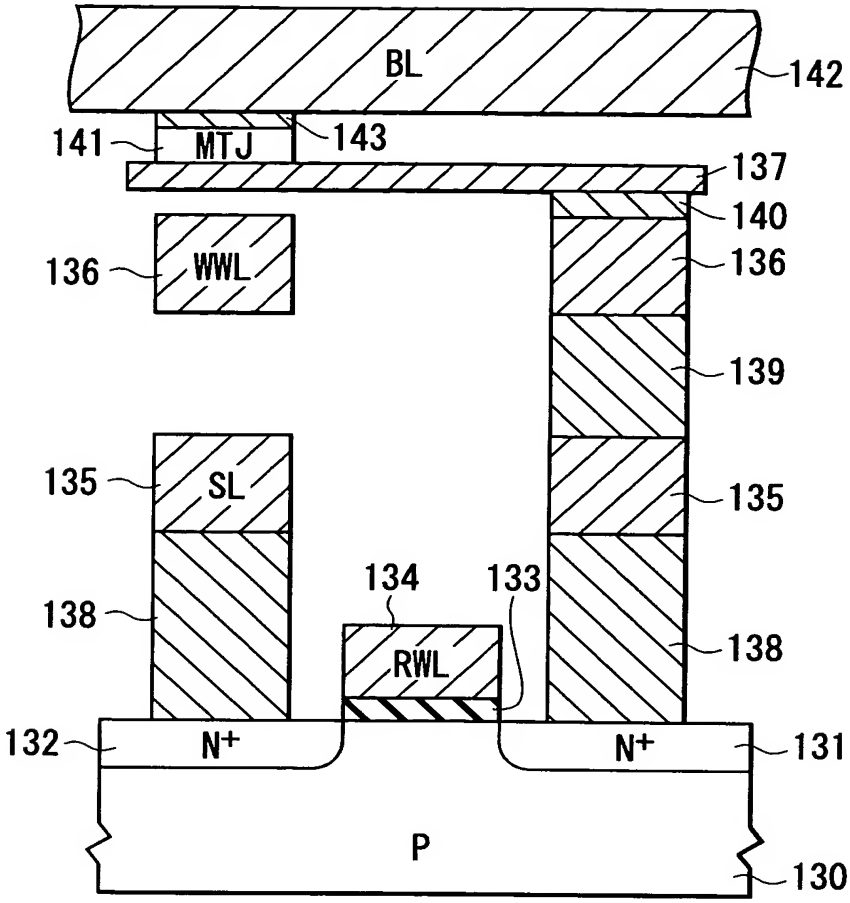

BL
142
141
MTJ
143
137
140
136
WWL
136
139
135
SL
135
134
133
138
RWL
138
132
N+
N+
131
P
130

FIG. 15

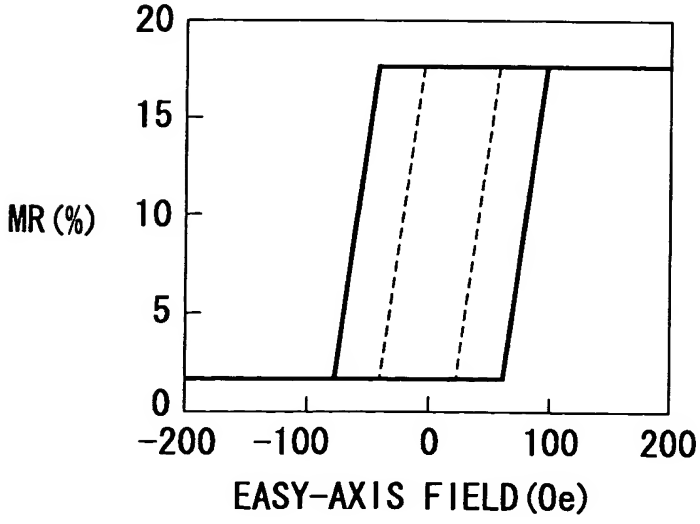
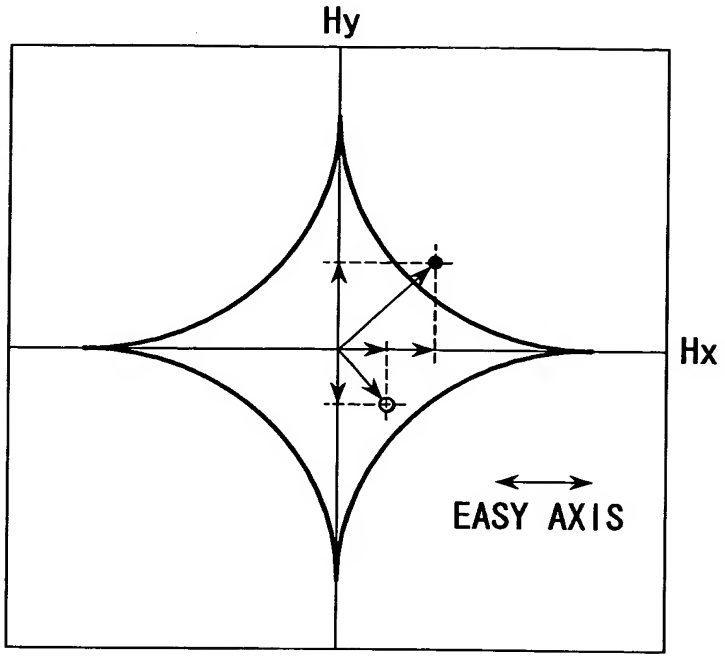

20
15
MR (%)
10
5
0
-200
-100
0
100
200
EASY-AXIS FIELD (Oe)

FIG. 16

FIG. 17


Hy
Hx
EASY AXIS

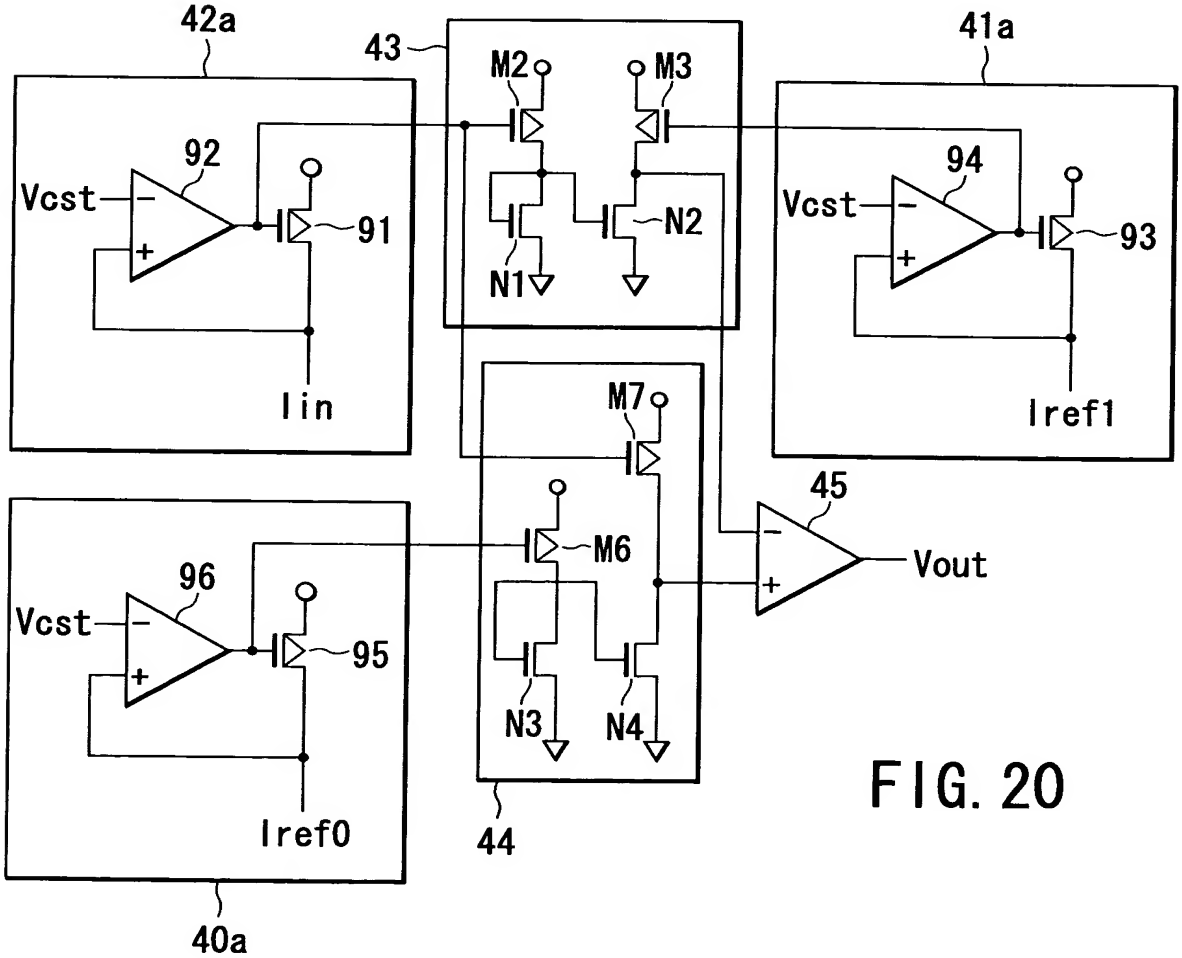

42a
43
41a
M2
M3
92
Vcst
91
N2
N1
94
Vcst
93
Iin
Iref1
M7
45
M6
Vout
96
Vcst
95
N3
N4
Iref0
44
40a

FIG. 20

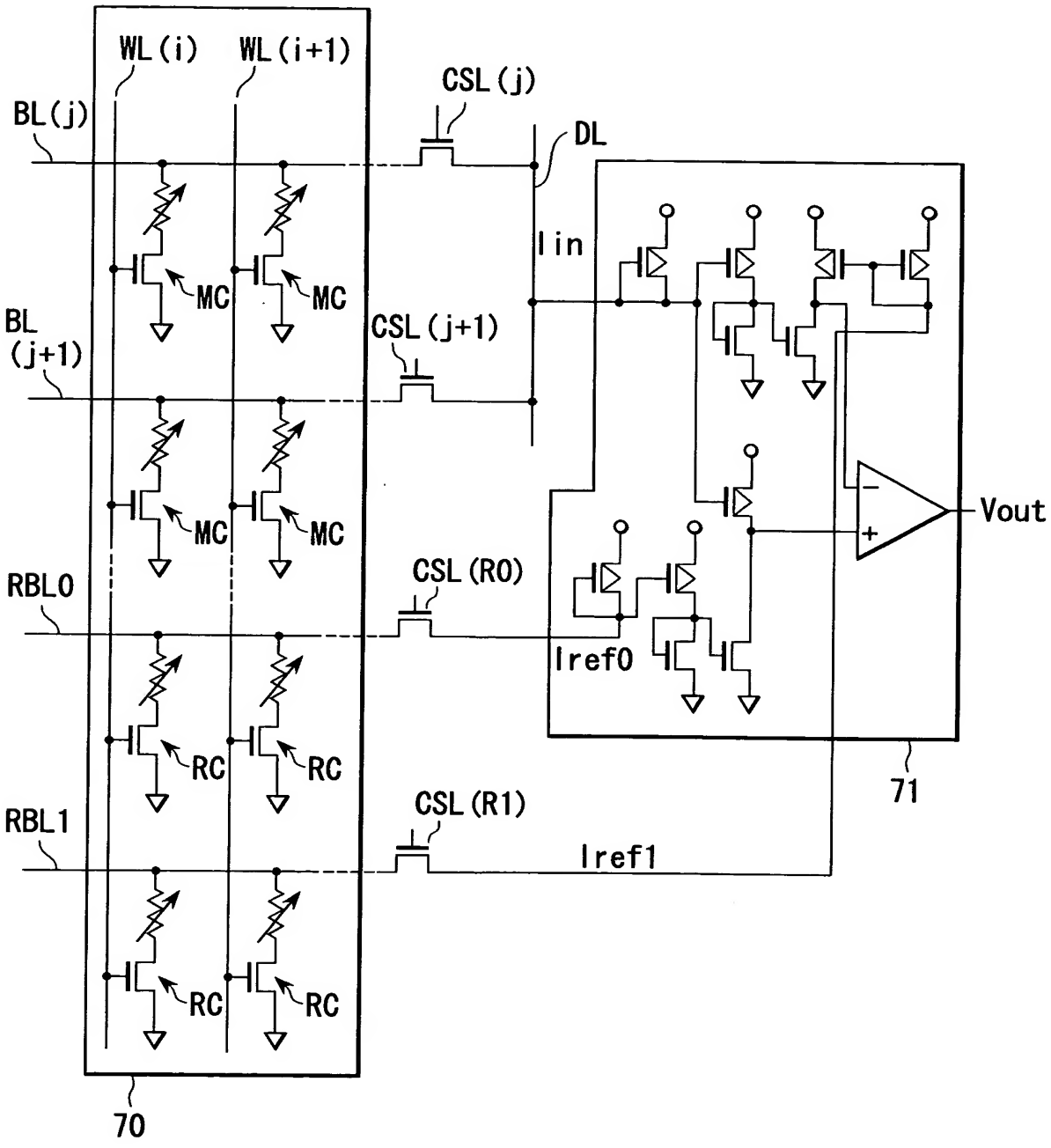

WL(i)
WL(i+1)
CSL(j)
BL(j)
DL
Iin
MC
MC
BL
(j+1)
CSL(j+1)
MC
MC
Vout
RBL0
CSL(R0)
Iref0
RC
RC
71
RBL1
CSL(R1)
Iref1
RC
RC
70

FIG. 18

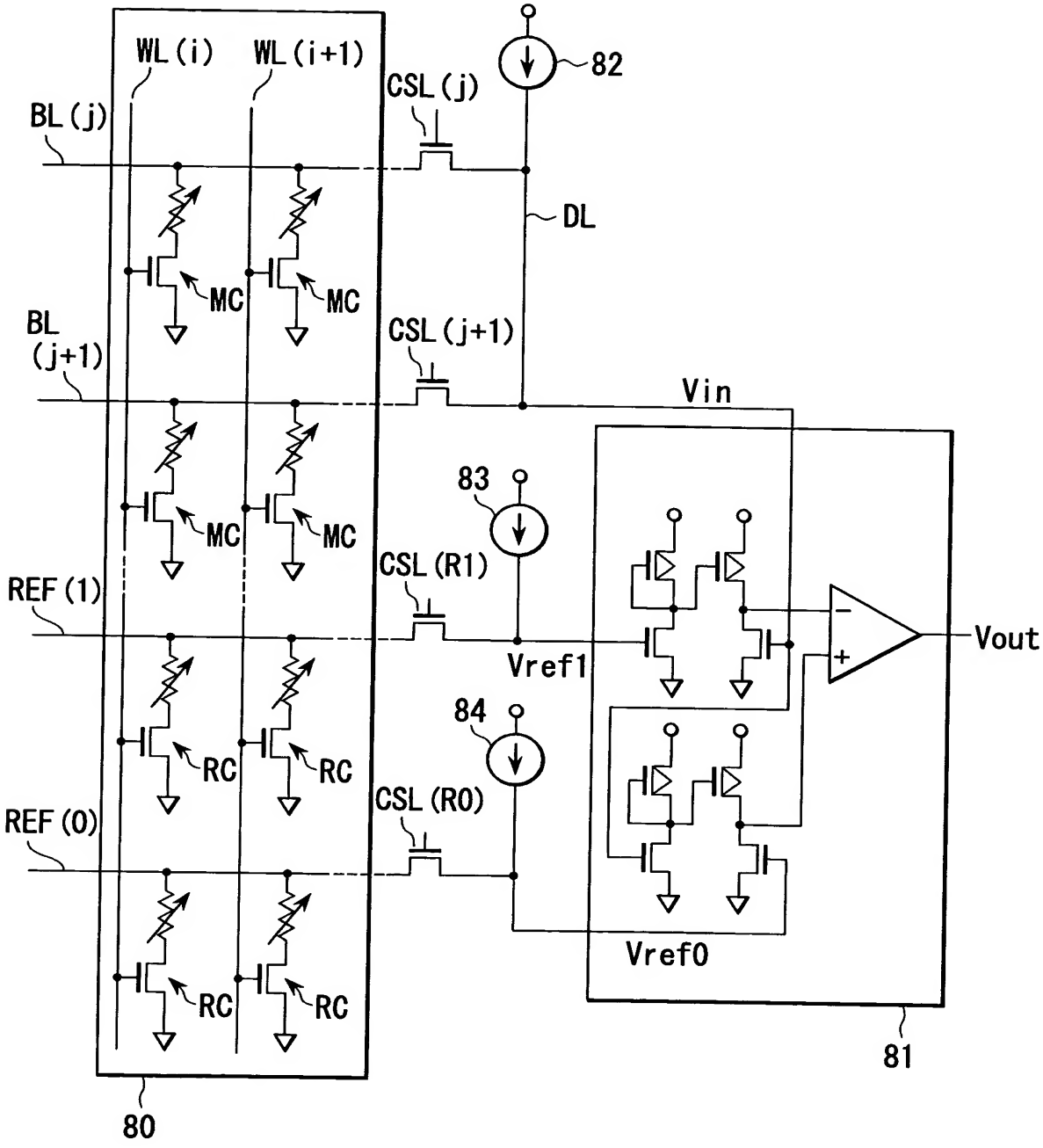

WL (i)
WL (i+1)
CSL (j)
82
BL (j)
DL
MC
MC
BL
(j+1)
CSL (j+1)
Vin
MC
MC
83
CSL (R1)
REF (1)
Vout
Vref1
84
RC
RC
CSL (R0)
REF (0)
Vref0
RC
RC
80
81

FIG. 19

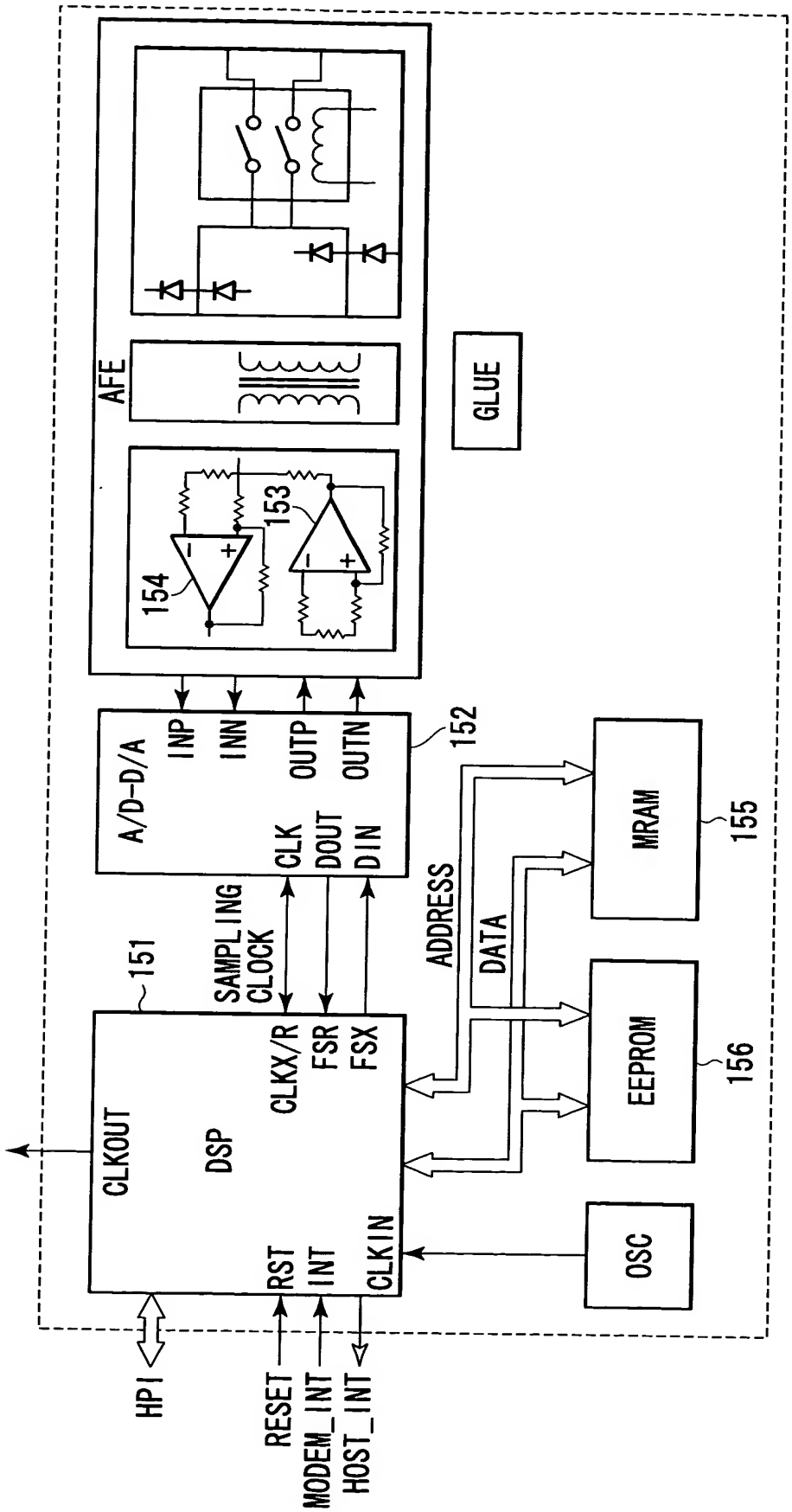

AFE
GLUE
154
153
A/D-D/A
INP
INN
OUTP
OUTN
CLK
DOUT
DIN
152
SAMPLING CLOCK
151
ADDRESS
DATA
MRAM
155
EEPROM
156
CLKOUT
DSP
CLKX/R
FSR
FSX
RST
INT
CLKIN
OSC
HPI
RESET
MODEM_INT
HOST_INT

FIG. 21

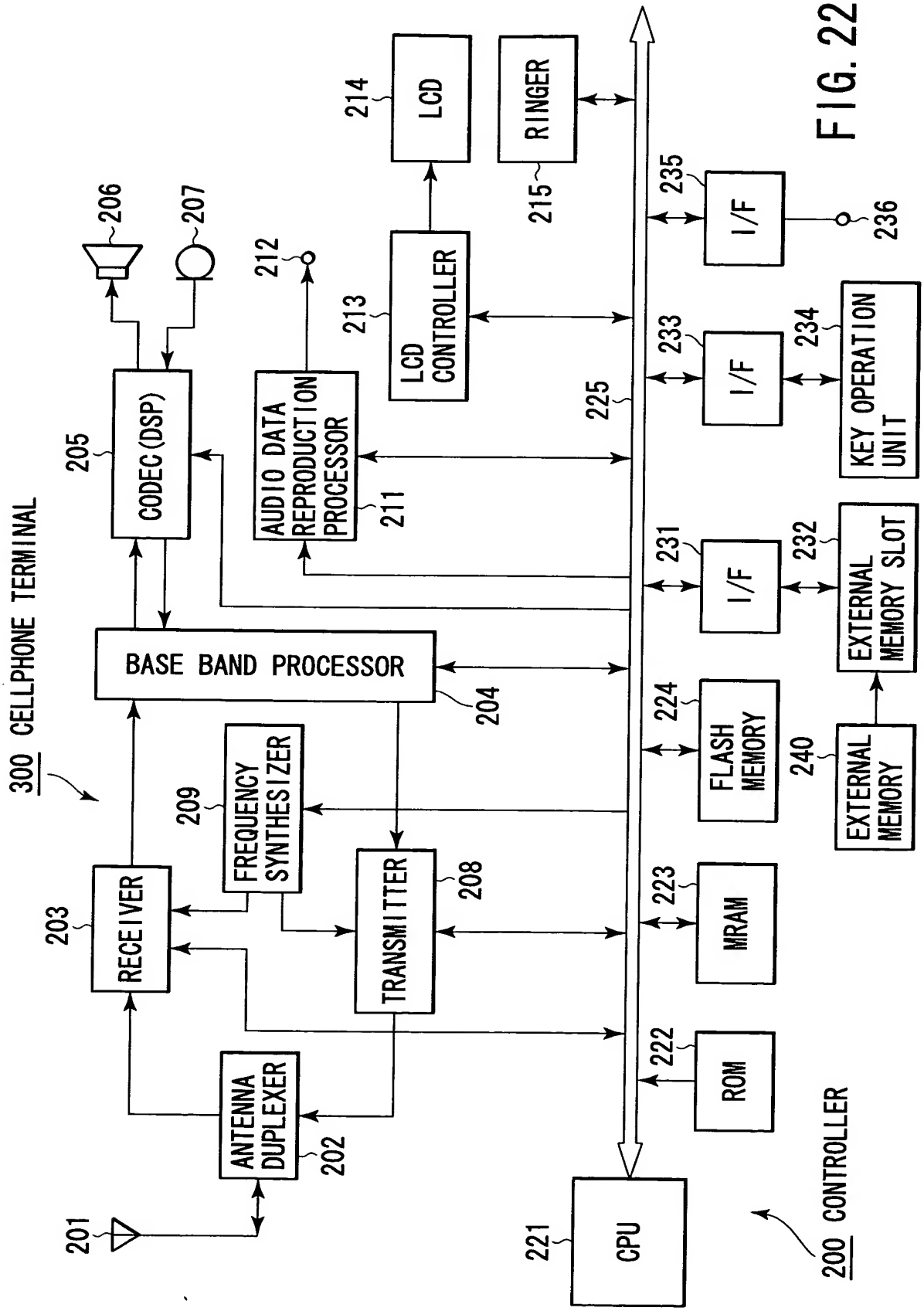

300 CELLPHONE TERMINAL
201
ANTENNA DUPLEXER
202
RECEIVER
203
BASE BAND PROCESSOR
204
CODEC (DSP)
205
206
207
FREQUENCY SYNTHESIZER
209
TRANSMITTER
208
AUDIO DATA REPRODUCTION PROCESSOR
211
212
LCD CONTROLLER
213
LCD
214
RINGER
215
225
I/F
231
I/F
233
I/F
235
EXTERNAL MEMORY SLOT
232
KEY OPERATION UNIT
234
236
FLASH MEMORY
224
EXTERNAL MEMORY
240
MRAM
223
ROM
222
CPU
221
200 CONTROLLER

FIG. 22

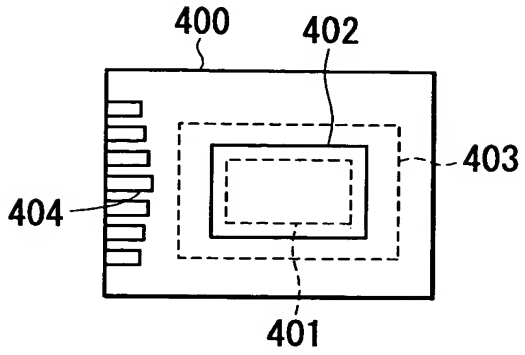


FIG. 23

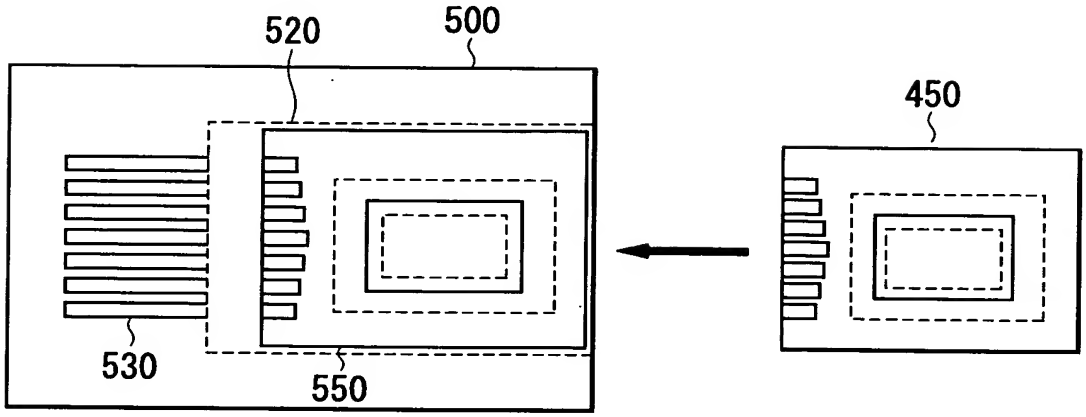
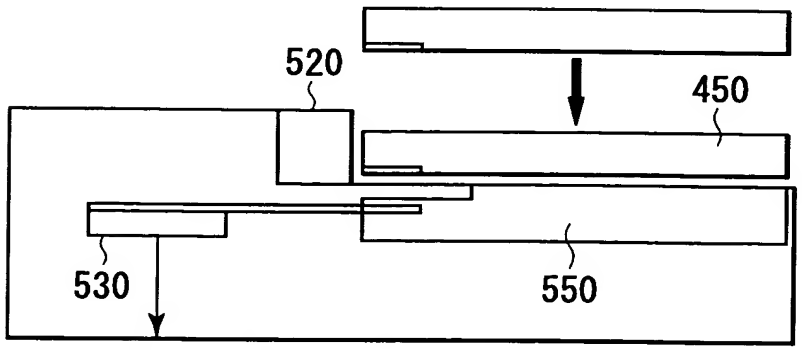


FIG. 24



TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 26

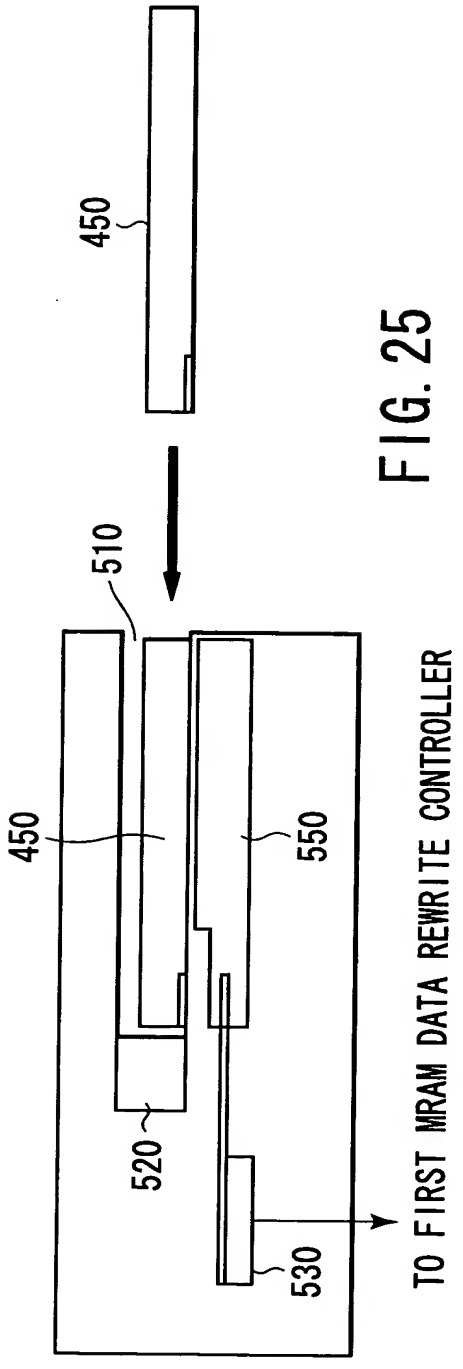

450
510
450
550
520
530
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 25

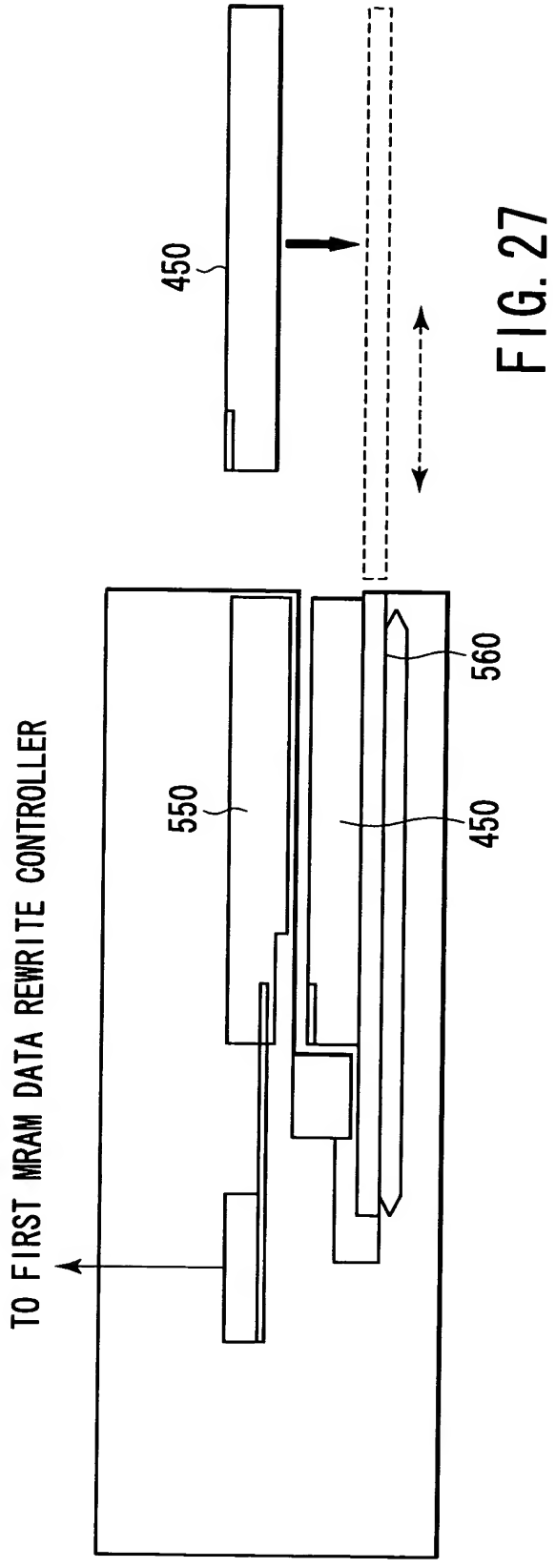

450
560
550
450
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 27